DOROS standard BPM system (BIDRS)

M. Gasior, SY-BI-IQ
v. 1/03/22

BPMSW aperture = 61 mm (warm 120 mm stripline)
BPMRA aperture = 49 mm (cryo 24 mm buttons)
BPMSA aperture = 81 mm (warm 120 mm stripline)

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-	New atetnuators	Old attenuators
Q1 P1 L	BPMSW.1L1.B1	CFB-UJ14-BIDRS1	BY01.UJ14	0x81FF 8 | 00	08:00:30:F6:81:FF socket ->: location ->	BY01.UJ14 3004/01 2119 0-0010	BY01 UJ14 A B1: socket #11 B2: socket #12	cable # attenuator # splitter #	11069 - 31 251 102	32 270 103	33 256 105	34 259 107	6	10
	BPMSW.1L1.B2							cable # attenuator # splitter #	11069 - 35 210 108	36 246 113	37 216 109	38 239 110	9	12
New 2022	BPMSW.1L1.B1_B BPMSW.1L1.B2_B	CFB-UJ14-BIDRS1B		0x818F	08:00:30:F6:81:8F	3004/03	no timing	SMA splitters just before the beam inputs						
Q2 P1 L	BPMS.2L1.B1 tilted 45 degrees !	CFB-UJ14-BIDRS2	BY01.UJ14	0x81FE 8 | 00	08:00:30:F6:81:FE socket ->: location ->	BY01.UJ14 3004/02 2119 0-0010	BY01 UJ14 A	cable # attenuator # splitter #	11069 - 23	24	25	26		
	BPMS.2L1.B2							cable # attenuator # splitter #	11069 - 27	28	29	30		
Q1 P1 R	BPMSW.1R1.B1	CFB-UJ16-BIDRS1	BY01.UJ16	0x8101 8 | 00	08:00:30:F6:81:01 socket ->: location ->	BY01.UJ16 1705/01 2137 0-0001	BY01 UJ16 A B1: socket #11 B2: socket #12	cable # attenuator # splitter #	11069 - 39 233 111	40 283 114	41 222 112	42 229 115	9	12
	BPMSW.1R1.B2							cable # attenuator # splitter #	11069 - 43 253 117	44 260 118	45 254 119	46 265 120	6	10
New 2022	BPMSW.1R1.B1_B BPMSW.1R1.B2_B	CFB-UJ16-BIDRS1B		0x8181	08:00:30:F6:81:81	1705/04	no timing	SMA splitters just before the beam inputs						
Q2 P1 R	BPMS.2R1.B1 tilted 45 degrees !	CFB-UJ16-BIDRS2	BY01.UJ16	0x8102 8 | 00	08:00:30:F6:81:02 socket ->: location ->	BY01.UJ16 1705/02 2137 0-0001	BY01 UJ16 A	cable # attenuator # splitter #	11069 - 47	48	49	50		
	BPMS.2R1.B2	FE exchanged on 21/08/18 (broken -13 V PS) new front-end with every 2nd top screw 3x6						cable # attenuator # splitter #	11069 - 51	52	53	1124282		

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v. 1/03/22

BPMSW aperture = 61 mm (warm 120 mm stripline)
BPMRA aperture = 49 mm (cryo 24 mm buttons)
BPMSA aperture = 81 mm (warm 120 mm stripline)

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-		New atetnuators	Old attenuators
							BST1, BST2 missing								
Q7 P1 L	BPMRA.7L1.B1	CFB-RR13-BIDRS1	BY01.RR13	0x81F9 8 | 00	08:00:30:F6:81:F9 socket ->	BY01.RR13 3110/01	BY01 RR13 A B1: socket #11	cable # attenuator #	11068 - 75 no attenuators	76	77	78			
					location ->	3110 U-3110	B2: socket #12	splitter #		splitters not in order, B1+B2 pairs 72+82, 70+85, 68+77, 67+71					
	BPMRA.7L1.B2				ETH by fibre, 8 sockets seen as one socket 3110/01 switch P3110-R-IP3-SHP1S-E1			cable # attenuator # splitter #	11068 - 79 no attenuators	80	81	82			
	### 7R1.B1: H- electrode problem ? ###						BST1, BST2 missing							### 7R1.B1: strange, low amplitude on H- ### spotted on 2/11/20 while analysing da	
Q7 P1 R	BPMRA.7R1.B1	CFB-RR17-BIDRS1	BY01.RR17	0x8107 8 | 00	08:00:30:F6:81:07 socket ->	BY01.RR17 3141/01	BY01 RR17 A B1: socket #11	cable # attenuator #	11069 - 95 no attenuators	96	97	1124288 !!!			
					location ->	3141 U-3141	B2: socket #12	splitter #		splitters not in order, B1+B2 pairs 80+96, 78+86, 75+81, 74+79					
	BPMRA.7R1.B2				ETH by fibre, 8 sockets seen as one socket 3141/01 switch P3141-R-IP3-SHP1S-E2			cable # attenuator # splitter #	11069 - 99 no attenuators	00	01	02			
							BST2 missing								
AFP P1 L ap. 81 mm	BPMSA.A6L1.B2	CFB-RR13-BIDRS2	BY03.RR13	0x819F 4 | 10	08:00:30:F6:81:9F socket ->	BY01.RR13 3110/01	BY01 RR13 A B2: socket #17	cable # attenuator #	11028 - 61	62	63	64		10 dB, installed by Marek	
					location ->	3110 U-3110		splitter #	no splitters						
	######## one BPM front-end ######## channels 5 - 8 disabled, CH config bits = "10" An "odd" left side BPM, so ID numbered from 0x100 - 0x61 = 9F (159)				ETH by fibre, 8 sockets seen as one socket 3110/01										
							BST1 missing								
AFP P1 R ap. 81 mm	BPMSA.A6R1.B1 The stripline inversed !!!	CFB-RR17-BIDRS2	BY01.RR17	0x8161 4 | 10	08:00:30:F6:81:61 socket ->	BY01.RR17 3141/01	BY01 RR17 A B1: socket #17	cable # attenuator #	11028 - 85	86 143	87 173	88 156	168	10 dB, installed by Marek	
					location ->	3141 U-3141		splitter #	no splitters						
	######## one BPM front-end ######## channels 5 - 8 disabled, CH config bits = "10" An "odd" right side BPM, so ID numbered from 0x61 (97)				ETH by fibre, 8 sockets seen as one socket 3141/01										

DOROS standard BPM system (BIDRS)

M. Gasior, SY-BI-IQ
v. 1/03/22

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-
Q1 P2 L	BPMSW.1L2.B1	CFB-UA23-BIDRS1	BY02.UA23	0x82FF 8 | 00	08:00:30:F6:82:FF socket ->	BY01.UA23 8905/05	BY02 UA23 B1: socket #2	cable # attenuator #	12060 - 70	71	72	73
					location ->	2218 R-0000	B2: socket #4	splitter #				
	BPMSW.1L2.B2		BPM cables in BY01				BST1 OK BST2 OK	cable # attenuator # splitter #	12060 - 74	75	76	77
Q1 P2 R	BPMSW.1R2.B1	CFB-UA27-BIDRS1	BY01.UA27	0x8201 8 | 00	08:00:30:F6:82:01 socket ->	BY01.UA27 1105/06	BY01 UA27 A B1: socket #3	cable # attenuator #	12060 - 78	79	80	81
					location ->	2239 R-0001	B2: socket #2	splitter #				
	BPMSW.1R2.B2					works with socket 04 !!!	BST1 missing BST2 OK	cable # attenuator # splitter #	12060 - 82	83	84	85
Q6 P2 R	BPM.6R2.B1	CFB-UA27-BIDRS2	BY04.UA27	0x8206 8 | 00	08:00:30:F6:82:06 socket ->	BY04.UA27 9708/02		cable # attenuator #	12061 - 26	27	28	29
New 2018					location ->	2239 R-0000		splitter #				
	BPMR.6R2.B2			### NEW sockets installed: 9708/03 - 06 ### 03 - BIDRC2 ### troubles to get socket 02 working, declaring a spare connection				cable # attenuator # splitter #	12061 - 30	31	32	33

DOROS standard BPM system (BIDRS)

M. Gasior, SY-BI-IQ
v. 1/03/22

BPLX aperture = 81 mm (warm 400 mm stripline)

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-
BBQ RR47 on demand gated	BPLX.D6R4.B1	CFB-UA47-BIDRS1	BY06.UA47 cables FE in RR47	0x8401 8 | 00	08:00:30:F6:84:01 socket -> location ->	BY05.UA47 8904/08 2439 U0-0001	no timing FE in the tunnel	cable # attenuator # splitter #		FE in the tunnel no connection to BPMs		
	BPLX.B6R4.B2				free sockets:	8905/05 .. 08		cable # attenuator # splitter #		system defined with "on demand gated" B1 and B2 striplines		
Q6 P4 L New 2018	BPMYB.6L4.B1	CFB-UA43-BIDRS1	BY08.UA43	0x84FA 8 | 00	08:00:30:F6:84:FA socket -> location ->	BY08.UA43 B603/05 2418 U0-0001		cable # attenuator # splitter #	14114 - 05	06	07	08
	BPMYA.6L4.B2							cable # attenuator # splitter #	14114 - 09	10	11	12
Q5 P4 R New 2018 dI/dt syst. A	BPMYA.5R4.B1	CFB-UA47-BIDRS2	BY05.UA47	0x8405 8 | 00	08:00:30:F6:84:05 socket -> location ->	BY05.UA47 8905/07 2439 U0-0001		cable # attenuator # splitter #	14091 - 38	39	40	41
	BPMYB.5R4.B2							cable # attenuator # splitter #	14091 - 42	43	44	45
Q6 P4 R New 2018 dI/dt syst. B	BPMYA.6R4.B1	CFB-UA47-BIDRS3	BY05.UA47	0x8406 8 | 00	08:00:30:F6:84:06 socket -> location ->	BY05.UA47 8905/08 2439 U0-0001		cable # attenuator # splitter #	14091 - 46	47	48	49
	BPMYB.6R4.B2							cable # attenuator # splitter #	14091 - 50	51	52	53

DOROS standard BPM system (BIDRS)

M. Gasior, SY-BI-IQ
v. 1/03/22

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-	New atetnuators	Old attenuators
Q1 P5 L	BPMSW.1L5.B1	CFB-USC55-BIDRS1	BY01.USC55	0x85FF 8 | 00	08:00:30:F6:85:FF old MCU socket -> location ->	BY03.USC55 1519/07 3524 1-0000	BY01 USC55 A B1: socket #11 B2: socket #12	cable # attenuator # splitter #	15082 - 38	39	40	41		
	BPMSW.1L5.B2					free sockets 1619/09..12	BST1 OK BST2 OK	cable # attenuator # splitter #	15082 - 42	43	44	45		
Q1 P5 R	BPMSW.1R5.B1	CFB-UJ56-BIDRS1	BY01.UJ56	0x8501 8 | 00	08:00:30:F6:85:01 socket -> location ->	BY01.UJ56 1307/01 2537 1-0000	BY01.UJ56 B1: socket #11 B2: socket #12 both on lower patch	cable # attenuator # splitter #	15082 - 46	47	48	49		
	BPMSW.1R5.B2						BST1 OK BST2 OK	cable # attenuator # splitter #	15082 - 50	51	52	53		

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M. Gasior, SY-BI-IQ
v. 1/03/22

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-
Q5 P6 L	BPMYA.5L6.B1	CFB-UA63-BIDRS1	BY02.UA63	0x86FB 8 | 00	08:00:30:F6:86:FB socket -> location ->	BY02 5304/06 2618 R-0001		cable # attenuator # splitter #	16054 - 80	81	82	83
New 2018												
	BPMYA.5L6.B2							cable # attenuator # splitter #	16054 - 84	85	86	87
Q5 P6 R	BPMYA.5R6.B1	CFB-UA67-BIDRS1	BY02.UA67	0x8605 8 | 00	08:00:30:F6:86:05 socket -> location ->	BY02 4806/06 2639 R-4804		cable # attenuator # splitter #	16055 - 04	05	06	07
New 2018												
	BPMYA.5R6.B2							cable # attenuator # splitter #	16055 - 08	09	10	11

DOROS standard BPM system (BIDRS)

DEV front-ends in UJ76 for reliability checks
SPARE front-end in TZ76

Location -> 2737 U1-0001
rack -> BY02

BPM	Device name	Rack	DOROS FE ID	FE MAC	ETH rack / sockets	Timing patch	Logging	Comments	
UJ76 system 1	CFB-UJ76-BIDRD1	BY03.UJ76	0x9701	08:00:30:F6:97:01	2011/01	-	TSTLHC.BPM.1R7.B?_DOROS	new FE	all with BPMSW geometry
UJ76 system 2	CFB-UJ76-BIDRD2	BY03.UJ76	0x9702	08:00:30:F6:97:02	2011/02	-	TSTLHC.BPM.2R7.B?_DOROS	new FE	
UJ76 system 3	CFB-UJ76-BIDRD3	BY03.UJ76	0x9703	08:00:30:F6:97:03	2011/03	-	TSTLHC.BPM.3R7.B?_DOROS	former RR77	
UJ76 system 4	CFB-UJ76-BIDRD4	BY03.UJ76	0x9704	08:00:30:F6:97:04	2011/04	-	TSTLHC.BPM.4R7.B?_DOROS	former UJ76	
						- two venti patches V1 - two venti patches V2			
TZ76 system 1	CFB-TZ76-BIDRD1	BY03.TZ76	0x97FF	08:00:30:F6:97:FF	7503/12	-	TSTLHC.BPM.1L7.B?_DOROS	spare front-end in TZ76	

DOROS standard BPM system (BIDRS)

M. Gasior, SY-BI-IQ
v. 1/03/22

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Location	BPM	Device name	Rack	DOROS FE ID active ch. | config bits	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-	New atetnuators	Old attenuators
Q1 P8 L	BPMSW.1L8.B1	CFB-UA83-BIDRS1	BY02.UA83	0x88FF 8 | 00	08:00:30:F6:88:FF socket -> location ->	BY02.UA83 H606/02 2818 U0-0001	BY02 UA83 A B1: socket #5 B2: socket #2	cable # attenuator # splitter #	18108 - 58	59	60	61		10
	BPMSW.1L8.B2		BPM cables in BY01				BST1 missing BST2 missing	cable # attenuator # splitter #	18108 - 62	63	64	65		10
Q1 P8 R	BPMSW.1R8.B1	CFB-UA87-BIDRS1	BY01.UA87	0x8801 8 | 00	08:00:30:F6:88:01 socket -> location ->	BY01.UA87 2205/04 2839 U0-0001	BY01 UA87 B B1: socket #3 B2: socket #4	cable # attenuator # splitter #	18108 - 66	67	68	69		9
	BPMSW.1R8.B2						BST1 missing BST2 missing	cable # attenuator # splitter #	18108 - 70	71	72	73		9
Q6 P8 L New 2018	BPMR.6L8.B1	CFB-UA83-BIDRS2	BY05.UA83	0x88FA 8 | 00	08:00:30:F6:88:FA socket -> location ->	BY05.UA83 2606/07 2818 U0-0001		cable # attenuator # splitter #	18108 - 10	11	12	13		
	BPMR.6L8.B2							cable # attenuator # splitter #	18108 - 14	15	16	17		
Q6 P8 R New 2018	BPM.6R8.B1	CFB-UA87-BIDRS2	BY06.UA87	0x8806 8 | 00	08:00:30:F6:88:06 socket -> location ->	BY07.UA87 J611/05 2839 U0-0001		cable # attenuator # splitter #	18109 - 14	15	16	17		
	BPM.6R8.B2							cable # attenuator # splitter #	18109 - 18	19	20	21		

DOROS standard BPM system (BIDRS)

SPS front-ends

Location	BPM	Device name	Rack	DOROS FE ID	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-	
SPS DOROS in BA5	BPMBV 518 aperture 83 mm	CFB-ECA5-BIDRS1 <---------- in fact this is H, with aperture 156 mm...	?	0x8A51	08:00:30:F6:8A:51 socket -> location ->	? 2325/01 0899 S1-2325		cable # attenuators	35008 - 50 4 x 10 dB / 5W	51	49	48	channels 1 .. 4
	BPMBH 520 aperture 156 mm							cable # attenuators	35008 - 57 4 x 10 dB / 5W	56	58	59	channels 5 .. 8
SPS DOROS crab BA6	BPMCA 61736	CFB-BA6-BIDRS1	BA60 RA1322	0x8A61	08:00:30:F6:8A:61 socket -> location ->	BA60 RA1321 2706/04 0873 R-0010		cable # attenuators	36030 - 43 4 x 10 dB / 5W	44	45	46	channels 1 .. 4
	BPMCA 61751 apertures 83.2 mm polynomial as for LHC BPMWI		polarity invertd in H as reported by Tom on 30/05/15					cable # attenuators	36030 - 47 4 x 10 dB / 5W	48	49	50	channels 5 .. 8
SPS TN testing in BA3 TN place holder for CHARM	as BPMSW	CFB-BA3-BIDRS1	BA30 RA 0334	0x8A31	08:00:30:F6:8A:31 socket -> location ->	BA30 RA 0334 0818/04 0870 R-0009	no timing		inputs not conencted		logged as BPMSW	ch.1 - 4: SPS.BPM_DOROS.SR301 ch.5 - 8: SPS.BPM_DOROS.SR302	SR = SpaRe
CHARM dry run		CFB-157-BIDRS1			08:00:30:F6:8A:3A socket -> location ->	6209/21 157-1-6209	range 6209/02 - 23						
CHARM irradiation		CFB-157-BIDRS2			08:00:30:F6:8A:3B socket -> location ->	7107/21 157-1-7107	range 7107/02 - 23						

DOROS standard BPM system (BIDRS)

DEV SPS front-ends

Location	BPM	Device name	Rack	DOROS FE ID	FE MAC	ETH rack / sockets	Timing patch		Cable H+	Cable H-	Cable V+	Cables V-	
									Cable H+ (ext)	Cable H- (int)	Cable V+ (up)	Cables V- (down)	BPM
SPS DOROS DEV	not conencted	CFB-HCA4-BIDRS1	?	0x8A41	08:00:30:F6:8A:41	?.HCA4	no timing	cable #	34059 - 58	57	59	60	BPCEH 41801
					socket ->	2317/03	<- free 2317/04	cable #	34059 - 62	61	63	64	BPCEV 41931
### FE not present ####					location ->	0921 S2-0001		cable #	34059 - 54	68	55	56	BPCEV 41705
SPS MOPOS DEV	MOPOS BPMs	CFB-HCA4-BIDRD1	HCA4 RA1217	0x9A41	08:00:30:F6:9A:41	?.HCA4	no timing	cabling dynamically changing					
					socket ->	1817/07							
### FE not present ####					location ->	0921 S2-0001							

DOROS standard BPM system (BIDRS)

DEV lab front-ends

Location	BPM	Device name	Rack	DOROS FE ID	FE MAC	ETH rack / sockets	Timing patch	Logging	Comments	
0866 R-0D02	labo system 1	CFB-866-BIDRD1	labo	0x9F01	08:00:30:F6:9F:01	0D02/04	labo			
0866 R-0D02	labo system 2	CFB-866-BIDRD2	labo	0x9F02	08:00:30:F6:9F:02	0D02/04	labo			
0866 R-0D02	labo system 3	CFB-866-BIDRD3	labo	0x9F03	08:00:30:F6:9F:03	0D02/04	labo			
0866 R-0D02	labo system 4	CFB-866-BIDRD4	labo	0x9F04	08:00:30:F6:9F:04	0D02/04	labo			
0866 R-0D02	labo system 5	CFB-866-BIDRD5	labo	0x9F05	08:00:30:F6:9F:05	0D02/04	labo			
0866 R-0D02	labo system 6	CFB-866-BIDRD6	labo	0x9F06	08:00:30:F6:9F:06	0D02/04	labo			
0866 1-0A17	labo system 7	CFB-866-BIDRD7	old labo	0x9F07	08:00:30:F6:9F:07	0A21/04	labo			
0866 1-0A17	labo system 8	CFB-866-BIDRD8	old labo	0x9F08	08:00:30:F6:9F:08	0A21/04	labo			
						all on the same socket				
						socket ->	0021/04			
						location ->	0866 1A-0017			
Storage 866	storage system 1	CFB-866-BIDRD16	labo	0x9F10	08:00:30:F6:9F:10	storage rack	storage	TSTLHC.BPM.SR1.B?_DOROS	all with BPMSW geometry	SR = SpaRe
Storage 866	storage system 2	CFB-866-BIDRD17	labo	0x9F11	08:00:30:F6:9F:11	storage rack	storage	TSTLHC.BPM.SR2.B?_DOROS		
Storage 866	storage system 3	CFB-866-BIDRD18	labo	0x9F12	08:00:30:F6:9F:12	storage rack	storage	TSTLHC.BPM.SR3.B?_DOROS		
Storage 866	storage system 4	CFB-866-BIDRD19	labo	0x9F13	08:00:30:F6:9F:13	storage rack	storage	TSTLHC.BPM.SR4.B?_DOROS		
Storage 866	storage system 5	CFB-866-BIDRD20	labo	0x9F14	08:00:30:F6:9F:14	storage rack	storage	TSTLHC.BPM.SR5.B?_DOROS		
Storage 866	storage system 6	CFB-866-BIDRD21	labo	0x9F15	08:00:30:F6:9F:15	storage rack	storage	TSTLHC.BPM.SR6.B?_DOROS		
Storage 866	storage system 7	CFB-866-BIDRD22	labo	0x9F16	08:00:30:F6:9F:16	storage rack	storage	TSTLHC.BPM.SR7.B?_DOROS		
Storage 866	storage system 8	CFB-866-BIDRD23	labo	0x9F17	08:00:30:F6:9F:17	storage rack	storage	TSTLHC.BPM.SR8.B?_DOROS		
						all on the same socket				
						socket ->	0406/01			
						location ->	0866 1-0406			
0866 1-0A01	dIdt dev #1	CFB-866-BIDRD32	labo	0x9F20	08:00:30:F6:9F:20	0A03/03	no timing		new 2018	

DOROS standard BPM system (BIDRS)

FE channel	Plane	Input
1	1	horizontal positive, BPM 1
2		horizontal negative, BPM 1
3	2	vertical positive, BPM 1
4		vertical negative, BPM 1
5	3	horizontal positive, BPM 2
6		horizontal negative, BPM 2
7	4	vertical positive, BPM 2
8		vertical negative, BPM 2

DOROS FE possible cofigurations:

- BPM 1/2 = B1/B2
- BPM 1/2 = B1/B1
- BPM 1/2 = B2/B2

timing 1: plane 1 (H): ch1 +, ch2 -
plane 2 (V): ch3 +, ch4 -

timing 2: plane 3 (H): ch5 +, ch6 -
plane 4 (V): ch7 +, ch8 -

BPM cable standard convention

cable no.	position	polarity	colour
n	exterior	H+	black
n + 1	interior	H-	red
n + 2	up	V+	yellow
n + 3	down	V-	white

Channel config bits

00 - all 1..8 channels enabled (most of the front-ends)
01 - channels 7..8 dispabled (no such a case in the S system, only one in the C system, FE for TCSPM.D4R7.B2)
10 - channels 5..8 dispabled (one BPM front-ends, in the S system only AFP FEs at P1)
11 - channels 3..8 dispabled (no such a case yet)

DOROS FE ID convention ("MAC MSB" + "MAC LSB" DIP switches on the FPGA board)

bit	length	function	value	description
15 ... 12	4	system ID	0	forbidden
			1	collimator BPMs
			2	development collimator BPMs
			8	standard BPMs
			9	development standard BPMs
11 ... 8	4	location	0	forbidden
			1	LHC point 1
			2	LHC point 2
			3	LHC point 3
			4	LHC point 4
			5	LHC point 5
			6	LHC point 6
			7	LHC point 6
			8	LHC point 8
			...	
			10	SPS --------> HEX unit ID starts with the sextand number, i.e. 41 = fist FE in sextant 4
			...	
			15	lab
7 ... 0	8	unit ID	0	forbidden ... FB - FC - FD - FE - FF - ### POINT ### - 01 - 02 - 03 - 04 - 05 ...
			1 ... 127	LHC right IP side
			255 ... 128	LHC left IP side (U2 negative numbers)

DOROS MAC addres = 08:00:30:F6: + FE ID

new CERN prefix: 80-D3-36, maybe to be used in the future

FE names	loc = location, e.g. USC55
	xx = sequential number 1, 2, 3, ...
CFB-loc-BIDRCxx	DOROS for collimator BPMs
CFB-loc-BIDRSxx	DOROS for standard BPMs
CFB-loc-BIDRDxx	DOROS for development

DOROS FE config bits ("FPGA SW" DIP switch on the FPGA board)

bit	length	function	value	description
7 ... 6	2	ch. in use	00	all 1..8 channels enabled (most of the front-ends)
			01	channels 7..8 dispabled (no such a case in the S system, only one in the C system, FE for TCSPM.D4R7.B2)
			10	channels 5..8 dispabled (one BPM connected to the front-end, in the S system only AFP FEs at P1)
			11	channels 3..8 dispabled (no such a case yet)
5 ... 2	4	installation year	modulo 16	---------->
1 ... 0	2	HW ver.	00	analog board with 1 dB step, separate OR and OS detectors, produced until 2018
			01	analog board with 0.5 dB step, common OR and OS detectors, produced from 2020
			10	reserved
			11	reserved

year	year bits
2016	0000
2017	0001
2018	0010
2019	0011
2020	0100
2021	0101
2022	0110
2023	0111
2024	1000
2025	1001
2026	1010
2027	1011
2028	1100
2029	1101
2030	1110
2031	1111
2032	0000